CLAIMS

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1. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

at least one void formed in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

2. A packaged semiconductor device as claimed in claim 1 wherein said at least one void extends into said underlying substrate.

3. A packaged semiconductor device as claimed in claim 1 wherein said at least one void extends from said first major face through said ~~electr~~ically conductive layer and said underlying substrate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. A packaged semiconductor device as claimed in claim 1 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. A packaged semiconductor device as claimed in claim 8 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

13. A packaged semiconductor device comprising:

a semiconductor chip;

a prepreg epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated prepreg layers, said prepreg laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated prepreg layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said prepreg epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated prepreg layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

14. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, wherein said void is characterized by a profile that varies across adjacent laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said varying profile so as to contact a portion of said laminate between said first and second major faces of said laminate.

15. A packaged semiconductor device as claimed in claim 14 wherein

said laminate includes a selected laminated layer and an adjacent laminated layer,

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said void extends from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said varying profile defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer.

16. A packaged semiconductor device as claimed in claim 14 wherein said varying profile is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer.

17. A packaged semiconductor device as claimed in claim 16 wherein said second value is larger than said first value.

18. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, including a selected laminated layer and an adjacent laminated layer, wherein

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said laminate includes at least one void formed therein so as to extend from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said void is characterized by a varying profile that defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said ledge portion into said underlying cavity so as to contact a portion of said laminate between said first and second major faces of said laminate.

19. A packaged semiconductor device as claimed in claim 18 wherein said selected laminated layer comprises a plurality of laminated layers.

20. A packaged semiconductor device as claimed in claim 18 wherein said adjacent laminated layer comprises a plurality of laminated layers.

21. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, wherein said void is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said varying cross-sectional area.

22. An encapsulated integrated circuit comprising:

a semiconductor die;

a printed circuit board conductively coupled to said semiconductor die, wherein said printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said printed circuit board so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void.

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23. A computer including at least one packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

24. An epoxy resin glass-cloth laminate comprising:

a first major face;

a second major face oriented substantially parallel to said first major face;

a plurality of laminated epoxy resin glass-cloth layers defining a portion of said laminate between said first and second major faces, wherein said laminate includes at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, and wherein said void is characterized by a profile that varies across adjacent laminated layers.

25. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein

said laminated layers include a selected laminated layer and an adjacent laminated layer,

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said void extends from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said varying profile defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer.

26. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein said varying profile is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer.

27. An epoxy resin glass-cloth laminate as claimed in claim 26 wherein said second value is larger than said first value.

28. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein said laminated layers comprise bismaleimide triazine resin.

29. An encapsulated integrated circuit comprising:

a semiconductor die;

a printed circuit board conductively coupled to said semiconductor die, wherein said printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

a bismaleimide triazine resin laminate, including a selected laminated layer and an adjacent laminated layer, and

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, wherein

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said laminate includes at least one void formed therein so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said adjacent laminated layer, and

said void is characterized by a varying profile that defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend through said void into said underlying cavity so as to form an adhesive bond with said bismaleimide triazine resin laminate, wherein said semiconductor die is supported by said bismaleimide triazine resin laminate, and wherein said encapsulant and said bismaleimide triazine resin laminate are arranged to enclose substantially all of said semiconductor die.

30. A method of encapsulating an integrated circuit comprising the steps of:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

encapsulating said semiconductor die and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

31. A method of forming an epoxy resin glass-cloth laminate defining a first major face and a second major face oriented substantially parallel to said first major face, said method comprising a process of laminating a plurality of epoxy resin glass-cloth layers such that said laminate includes at least one void formed therein extending from one of said major faces through a plurality of said laminated layers, and such that said void is characterized by a profile that varies across adjacent laminated layers.